REMARKS/ARGUMENTS

The foregoing amendment and the following arguments are provided to impart precision to the claims, by more particularly pointing out the invention, rather than to avoid prior art.

35 U.S.C. § 112 Rejections

Examiner rejected claims 7-9 under 35 U.S.C. § 112, first paragraph, as failing to comply with the written description requirement. The Examiner asserts that claim 7 includes subject matter which was not described in the specification in such a way as to reasonably convey to one skilled in the relevant art that the inventor, at the time the application was filed, had possession of the claimed invention.

Specifically, the Examiner asserts that the phrase "a gate dielectric layer disposed superjacent the curvilinear recess and superjacent a portion of a top surface of the substrate," as found in claim 7, is not supported by the disclosure. However, Figures 19-22 show a gate dielectric 711 disposed superjacent the curvilinear recess and superjacent a portion of a top surface of the substrate, as is recited in claim 7. The limitation of claim 7 is therefore supported by the specification, and Applicant requests the removal of this rejection.

35 U.S.C. § 102 Rejections

Examiner rejected claims 4-6 under 35 U.S.C. § 102(a) as being anticipated by U.S. Patent No. 5,918,134 (hereinafter "Gardner").

Claim 4 includes a limitation of wherein an extension of the source/drain terminals extends to approximately a junction of the tapered sidewalls and the

bottom portion of the recess. Gardner does not disclose such a limitation, and therefore does not anticipate claim 1.

Specifically, Gardner discloses a transistor including lightly doped drain (LDD) regions 130. The LDD regions 130 are formed before a channel dielectric 126 is removed from a channel region 106 (Col. 6, lines 17-54). The LDD regions 130 therefore extend underneath the bottom portion and past the sidewalls of the gate dielectric 132 (See Figs. 8-10). Therefore, the LDD regions 130 extend past a junction of the bottom portion and the sidewalls of the gate dielectric 132, and Gardener does not disclose the cited limitation. As a result, claim 1 is not anticipated by Gardener.

Claims 2-3 depend from claim 1, and therefore include all the limitations of claim 1. Since claim 1 is not anticipated by Gardener, claims 2-3 are also not anticipated by Gardener.

35 U.S.C. § 103(a) Rejections

Examiner rejected claims 1-3 under 35 U.S.C. § 103(a) as being unpatentable by U.S. Patent No. 6,303,448 (hereinafter "Chang") in view of U.S. Patent No. 4,939,100 (hereinafter "Jeuch").

Claim 1 includes a limitation of wherein an extension of the source/drain regions extends to approximately a junction of the vertical sidewalls and the bottom portion of the recess. Neither Chang nor Jeuch include such a limitation. As a result, claim 1 is patentable over Chang and Jeuch.

Chang discloses a method for fabricating elevated source and drain structures on a substrate. Specifically, Chang discloses LDD regions 66 that are implanted before the spacers 68 are formed (Col. 5, lines 1-33). As can be seen in Figure 6 of Chang, the LDD regions 66 are formed below the spacers 68 and

extend past the bottom of the gate oxide layer. As a result, Chang does not disclose the cited limitation of claim 1.

Jeuch discloses a process for the production of a transistor with a rising substrate/gate dieletric interface. As can be seen in Figure 5I, a transistor 40 includes two doped zones 64 and 66 comprising the transistor source and drain (Col. 7, lines 36-46). The zones 64 and 66 are formed with one implantation, and do not include extensions. Further, the zones 64 and 66 do not extend to the junction of the sidewalls and the bottom of the silica layer 56. As a result, Jeuch does not disclose the cited limitation of claim 1.

Since neither Chang nor Jeuch disclose the cited limitation, claim 1 is patentable over Chang and Jeuch. Claims 2-3 depend from claim 1, and therefore include all the limitations of claim 1. Since claim 1 is patentable over Chang and Jeuch, claims 2 and 3 are also patentable over Chang and Jeuch.

CONCLUSION

Applicants respectfully submit the present application is in condition for allowance. If the Examiner believes a telephone conference would expedite or assist in the allowance of the present application, the Examiner is invited to call Arlen M. Hartounian at (408) 720-8300.

Authorization is hereby given to charge our Deposit Account No. 02-2666 for any charges that may be due.

Respectfully submitted,

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